EEPROM WITH REDUCED MANUFACTURING COMPLEXITY

ABSTRACT OF THE DISCLOSURE

A semiconductor device (200) comprising a semiconductor substrate (210) having source and drain regions (530, 540) located in the semiconductor substrate (210) and having similar doping profiles, wherein a channel region (550) extends from the source region (530) to the drain region (540). The semiconductor device (200) also comprises a dielectric layer (230) located over the source and drain regions (530, 540), the dielectric layer (230) having first and second thicknesses (T_1, T_2) wherein the second thickness (T_2) is substantially less than the first thickness (T_1) and is partially located over the channel region (550). The semiconductor device (200) also comprises a gate (510) located over the dielectric layer (230) wherein the second thickness (T_2) is located between an end (515) of the gate (510) and one of the source and drain regions (530, 540).